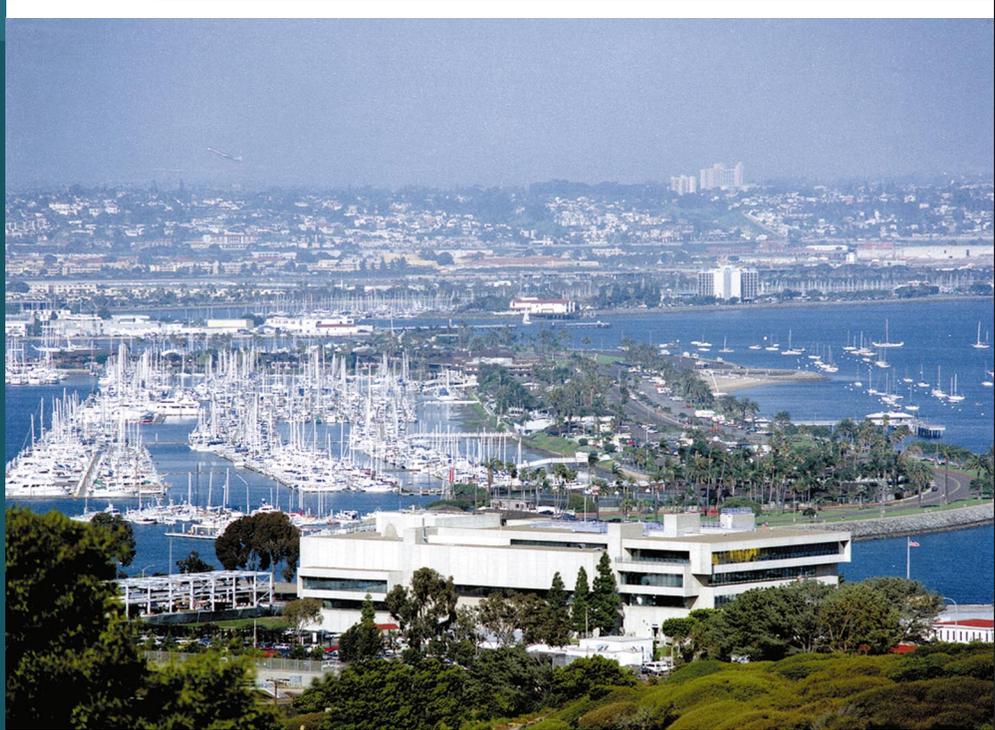


ON POINT



*High Performance
Computing News
from SSC San Diego*

High Performance Computing DoD Distributed Center

SSC San Diego is one of the original Department of Defense High Performance Computing Modernization Program (DoD HPCMP) sites. Established in 1993 and located at the Point Loma complex in San Diego, the SSC San Diego Distributed Center (DC) operates both classified and unclassified high performance computing (HPC) facilities in support of the computational science needs of the general engineering and science staff at the Center. The special focus of the DC is on requirements for command and control software development and for embedded signal and image processing surveillance applications research and development. The DoD HPCMP has funded the majority of the costs of establishing the SSC San Diego DC and has provided several increments of funding to upgrade the systems. The most recent upgrade began with DoD approval of a 1997 SSC San Diego proposal to leapfrog current HPC technologies in conformance with the Navy's Information Technology for the 21st Century (IT-21) and the DoD's 2010 visions. DoD funds were awarded to SSC San Diego to acquire scalable, parallel HPC systems that incorporated commodity, 64-bit Intel Architecture (IA-64) processors and that supported the option of running the Windows NT operating system. A competitive contract was awarded in 1998 to Hewlett-Packard (HP) to deliver these systems. As the development of the IA-64 processor was delayed, interim RISC-processor UNIX (only) systems were acquired to replace aging systems in the DC.

The two HPC facilities at SSC San Diego each include HP V2500 scalable parallel systems with 16 PA-RISC processors operating at 440 MHz and with 24-GB memory. Additionally, each facility includes EMC disk and HP/STK tape storage subsystems connected to the HP V2500 systems via Fibre Channel links and featuring Veritas hierarchical storage-management software to automatically handle all data archival and backup demands. The SSC San Diego DC is currently configured with 600-GB disk capacity and 10.5-TB robotic tape storage.

The latest upgrade of the SSC San Diego DC is scheduled for November 2000. This upgrade will add the newest Hewlett-Packard HPC system—the HP Superdome—to both the classified and unclassified facilities. Each Superdome system will be configured with 48 PA-RISC processors operating at 550 MHz with 48-GB memory. The Superdome machines will be connected to the existing storage subsystems via a Fibre Channel switch, along with the existing V2500 systems. While awaiting commercial availability of IA-64 HPC (McKinley) processors, SSC San Diego acquired small Intel-based WindowsNT servers to support local algorithm development efforts. Intel Xeon (IA-32) based HP Netservers were acquired in 1998, and Intel Itanium (IA-64) based servers will be delivered in 2001.

Each of the SSC San Diego DC HPC systems is connected to campus-wide, internal high-capacity networks. These systems connect, respectively, to the classified and unclassified OC-12c (622 Mb/s) asynchronous transfer mode (ATM) optical network backbones that link all of SSC San Diego's major sites and facilities. Together, these computing systems and networks provide the SSC San Diego scientific and engineering community with a state-of-the-art HPC environment to support Navy and DoD programs. These programs span the Department of Navy mission areas of command and control, communications, and surveillance, as well as a number of other technologies and Navy leadership areas.

SSC San Diego is also a principal developer of the Defense Research and Engineering Network (DREN). DREN has been a major node on the nationwide, high-speed network since its inception. SSC San Diego's networking role for the DoD provides technical leadership in implementing high-bandwidth links among all HPCMP sites and to many other DoD science and technology and development, test, and evaluation locations. The DREN node at SSC San Diego provides both secure and unclassified ATM OC-12c high-capacity connectivity that allows external DoD users to access the local distributed center systems. The DREN node also permits the Center's own research, development, test, and evaluation personnel to access other DoD HPC facilities.

The integration of these DC systems and networks in the SSC San Diego HPC environment supports both Navy-specific and Defense-wide mission areas. This integration allows us to join with the other DCs and the Major Shared Resource Centers in applying computational science to technical challenges and systems throughout the DoD. The resulting contributions have proven to be very valuable to SSC San Diego, to the Navy's research community, and to the broader DoD Science and Engineering (S&E) and Test and Evaluation (T&E) communities.

Access to SSC San Diego's DC systems is available to all DoD employees and DoD contractors engaged in research, development, test, and evaluation under rules specified by the DoD HPC Modernization Program Office. Access requires submission of a completed DoD account application to the appropriate DoD approval authority. The form and additional information may be obtained from the HPCMP World Wide Web site at <http://www.hpcmo.hpc.mil/>. Additional details about the SSC San Diego DC can be found at <http://www.sscsd.hpc.mil/dod/>.



**SSC San Diego
scientists and engineers have
been using local HPC capabilities
as well as those available at other DoD
HPCMO centers to solve complex problems for
the Navy and DoD in our primary charter areas of
command and control, communications, and surveillance
and in six other technical leadership areas assigned to us by
the Navy. The following seven success stories (to be detailed in the
forthcoming “High Performance Computing Contributions to DoD
Mission Success, 2000”) highlight SSC San Diego’s ability to deliver timely
solutions to complex military problems through the use of high performance
computing and networking.**

State-of-the-Art Electromagnetic Design Software and Virtual Prototyping: Affordable Technology for the Warfighter

Dr. C. W. Manry, Jr. and Dr. J. W. Rockway, SSC San Diego

HPC Computer Resource: IBM SP2 (U.S. Army Engineer Research and Development Center [ERDC] Major Shared Resource Center [MSRC]), SGI Origin 2000 (Aeronautical Systems Center [ASC] MSRC)

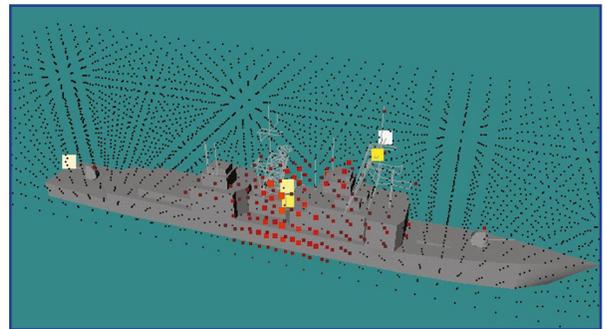
Research Objective: Develop Electromagnetics Interactions Generalized (EIGER), a state-of-the-art electromagnetic (EM) design software that can take advantage of HPC resources for future integrated topside designs for naval vessels. Modern software design and HPC resources offer the warfighter the best communication system concepts and performance to achieve the Joint Warfighting Capability Objectives and to retain superior command, control, communications, computers, intelligence, surveillance, and reconnaissance (C4ISR) capabilities. New technologies in composite structures, multifunction antennas, and electronically steered arrays are creating new challenges in design and evaluation of future communication systems. Through the use of EIGER and HPC resources, communication systems are now being designed, evaluated, and tested with increased accuracy and improved productivity.

Methodology: The key to EIGER development was to take essential physics properties and mathematical operators and cast them into a wide encompassing and general framework. Using this framework in conjunction with generalized object-oriented programming has led to a code of unprecedented application to a wide variety of electromagnetic problems and technologies. EIGER was in part developed as one of the High Performance Computing Modernization Program (HPCMP) Common High Performance Computing Software Support Initiative (CHSSI) Computational Electromagnetics and Acoustics (CEA) efforts with significant leveraging of funds from the Department of Energy and other government agencies. The EIGER CHSSI CEA project was initiated in April of FY 96 to focus on HPC aspects of this tool suite.

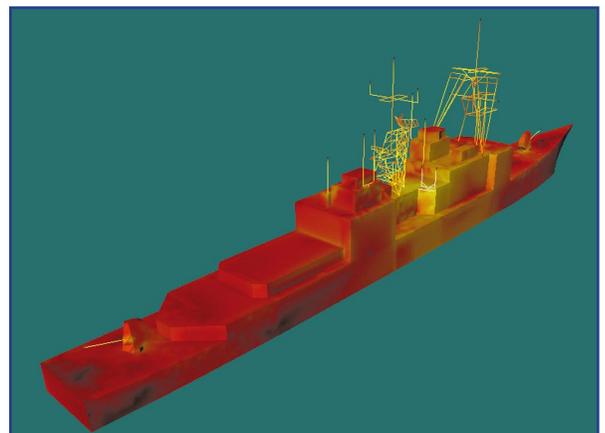
Results: The CHSSI EIGER project has resulted in a scalable and efficient code for government laboratories and industry to use in electromagnetic design. This code has been used with HPC resources to examine performance for the Navy's Advanced Enclosed Mast/Sensor and Low observable Multifunction Stack (LMS) Advanced Technology Demonstration programs. The complexity of these simulations required the use of huge amounts of CPU time and the granting of an FY 99 to FY 00 HPCMP Challenge status to the EIGER CHSSI development team. The large block of CPU time allowed the EIGER team to examine problems in greater detail and accuracy than ever previously attempted. In FY 99, over 160,000 CPU hours on an IBM SP2 were used in support of these and various other Navy programs.

Significance: The topside of a modern naval surface combatant is a sophisticated assortment of weapons, EM radiators, and other hardware. Large numbers of antennas, transmitters, and receivers are required to meet radar, information warfare, and communication requirements. An increasing inventory of EM systems is constantly being added to meet requirements for more communications capability with greater imagery and data-transfer capacity. The goal is to provide the warfighter at sea with ability to meet the Joint Warfighting Capability Objectives, which include information superiority and precision force. Designing and optimizing a complex EM environment is slow, expensive, and error-prone. Eighty percent of the "affordability" decisions are made before a detailed design is available for a new platform. The design tool set must provide a "total" integrated topside analysis in a cost-effective and timely manner. Advanced computational, visualization, and optimization tools that exploit HPC capabilities are critical to these required design tools. The computational electromagnetic framework EIGER provides this capability for virtual prototyping.

This work was done jointly with R. M. Sharpe and N. Champagne, Lawrence Livermore National Library, Berkeley.



Current on a Spruance-class destroyer due to a midship excited whip antenna at 10 MHz when using a "Hot" color-map. White indicates largest current values, and black indicates the smallest current values. Computed in 1 hour with 128 processors on IBM SP2, at the ERDC MSRC.



Nearby electric fields due to midship excited whip antenna at 10 MHz done to assess electromagnetic radiation hazards to personnel, fuel, and ordnance. Size and color of the sample points represent the value of the electric field at that point. Computed in 1 hour using 128 processors on IBM SP2 at the ERDC MSRC.

Scalable Sensor Modeling

Dr. M. E. Inchiosa and Dr. A. R. Bulsara

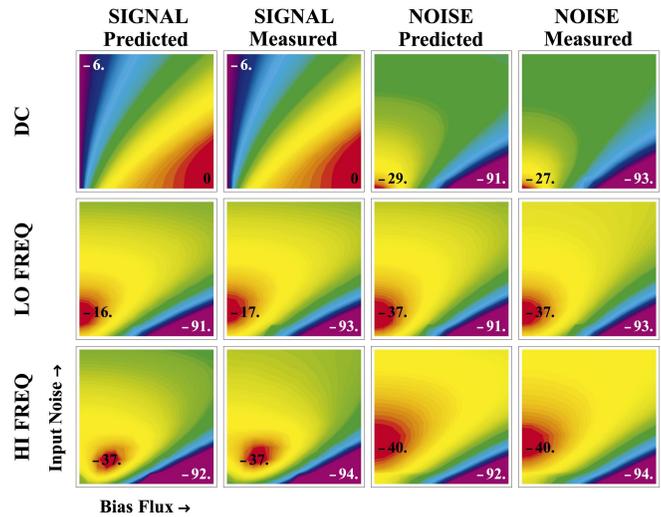
HPC Computer Resource: Cray T3E (ERDC and Naval Oceanographic Office [NAVO] MSRCs), SGI Origin 2000 (ASC MSRC), HP Exemplar SPP-1600 (SSC San Diego DC)

Research Objective: Develop scalable, portable HPC software for modeling nonlinear sensor arrays. Use the software developed to then design improved nonlinear sensors that exploit recent advances in nonlinear dynamics research.

Methodology: Nonlinear sensor arrays subject to random and deterministic signals and noise are modeled by systems of stochastic differential equations. Using Monte Carlo methods, the software solves such systems of equations to high accuracy. Structuring the solver to exploit coarse-grained parallelism results in highly scalable parallel performance, boasting 95% efficiency when scaled to 128 processing elements. This approach provides outstanding performance on all current parallel architectures: distributed memory, shared memory, and non-uniform memory access (NUMA). The code uses the modern features of FORTRAN 90/95 to achieve a modular, flexible design. Use of the industry-standard Message Passing Interfaces (MPI) library for parallelization ensures cross-platform portability across the computing spectrum from Windows-based workstations to Unix-based supercomputers.

Results: This new approach produced well-documented, standards-based, extensible software with graphical user interface (GUI)-based parameter entry and automated scientific visualization output. The developed code demonstrates high parallel scalability and portability. This software package allowed confirmation and evaluation of new modes of operating magnetic sensors based on arrays of superconducting quantum interference devices (SQUIDs). This new software promises improved magnetometers with greater noise tolerance and sensitivity, impacting surveillance, reconnaissance, and mine detection.

Significance: The significance of improving magnetic sensors is truly wide-ranging. Sensors based on this research may aid the warfighter by detecting underwater targets at greater range. Dual-use applications include airport baggage scanners for explosives and drug detection. Switching from traditional linear sensor modalities to nonlinear dynamic ones may also reduce transducer cost and result in simpler SQUID controller electronics. The software, developed with CHSSI Computational Electronics and Nanoelectronics (CEN) funding, allows verification of analytical approximations, and the knowledge we have gained leads toward development of nonsensor applications (e.g., novel transmitter/receiver active antenna arrays). Such applications impact a wide range of warfighting capabilities such as information superiority, precision force, combat identification, and joint theater missile defense.



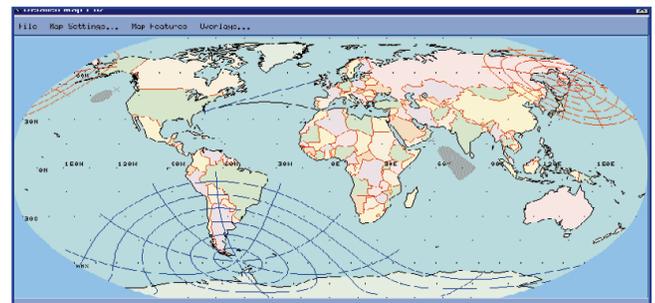
Signal and noise power output of a novel SQUID-based magnetic sensor, measured at three frequencies. The theoretically predicted results are verified by their excellent agreement with measured values from HPC-based numerical simulations.

World Wide to Regional Mapping Engine

L. McCleary

HPC Computer Resource: HP V2500 (SSC San Diego DC)

Research Objective: Develop a software mapping engine that can be used to display maps ranging in scale from worldwide to highly detailed regional areas. The data input must include all Vector Product Format (VPF) data from the National Imagery and Mapping Agency (NIMA). The software must be able to produce maps in multiple projections at any desired center point and must be able to correctly handle regions that encompass the dateline and/or poles. Additionally, the software must provide a basic set of overlay items and provide a means for users to geospatially register overlay symbology.



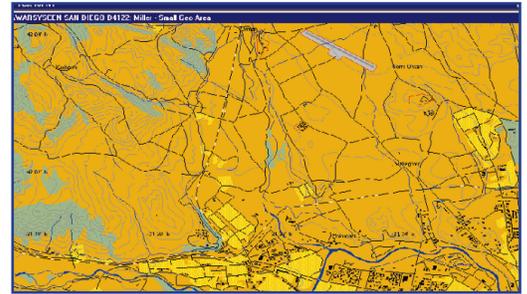
World view using Robinson Projection with Overlay Objects and Caricature Map Draw Module.

World Wide to Regional Mapping Engine (continued)

Methodology: To satisfy the research objectives, uniquely sophisticated algorithms have been developed. The resulting implementation has been developed in highly portable ANSI C that can be ported to a variety of Unix platforms, as well as Windows. Extensive testing must be performed on newly emerging VPF data. The capability needs to be accessible either as an embeddable system or in a client server mode.

Results: The actual software package is known as the Caricature Map Draw Module (MDM), which has been structured as a GUI independent library package. Extensive testing has proven that the algorithms are extremely robust in producing worldwide maps, including detailed areas at any region of the earth. Twenty one projections have been implemented to provide for a diversity of user applications. Overlay objects include great circle lines, rhumb lines, range rings, and satellite footprints. Implementation and testing has been performed on Sun, HP, and SGI machines, as well as on Windows NT and Windows 98. In addition, a Java client has been developed that can communicate with the server to retrieve and display MDM maps.

Significance: As a government-owned system, this software has proven to be extremely reliable and flexible in meeting the requirements of numerous DoD applications for organizations within the Navy, Army, Marine Corps, Joint Staff, and the National Reconnaissance Organization (NRO).



Detailed view using VPF Level 2 Data and Caricature Map Draw Module.

Data Distribution Environment for Signal-Processing Applications on Parallel Architectures

P. P. Partow and D. M. Cattel

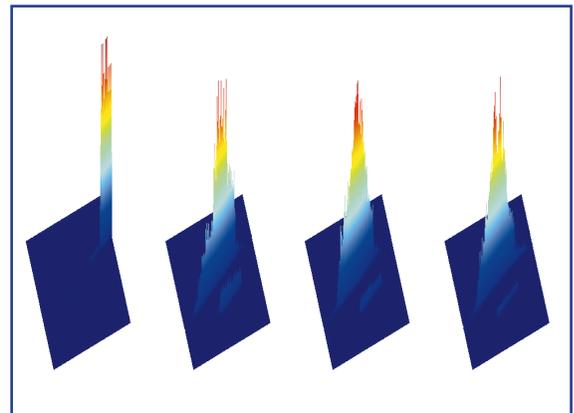
HPC Computer Resource: HP V2500 (SSC San Diego DC)

Research Objective: Develop a portable version of the SSC San Diego Scalable Programming Environment (SPE) and provide versions for various HPC systems and networks of workstations. DoD-embedded signal-processing applications are currently developed as conventional sequential programs and then rewritten as parallel programs for a specific embedded architecture. The SPE provides a way to develop scalable, parallel signal- and image-processing applications that can, by simple recompilation, be ported to various HPC architectures and ultimately to embedded systems. The concepts have been proven on an Intel Paragon and are in production use on the Hewlett-Packard V2500 at the SSC San Diego DC.

Methodology: The SPE is intended to be used for real-time signal processing and so has been implemented as an efficient environment for building applications in a modular, flexible scalable manner. The SPE handles the myriad complicated details of scalable parallelism so programmers can concentrate on signal-processing issues. The SPE has been successful not only in providing transparent scalability for users, but also in encouraging good software engineering practices such as modularity, well-defined interfaces, and rapid prototyping of parallel programs. The SPE was originally developed for a specific project funded by the Office of Naval Research, using the Intel Paragon at the SSC San Diego DC. Since that time, the Message Passing Interface (MPI) standard has become widely adopted as a low-level method of making parallel message passing programs portable to multiple HPC platforms. By taking advantage of the portability of MPI, the SPE has been made much more portable so that signal-processing applications may be quickly ported to new hardware architectures.

Results: Under the DoD HPC MP CHSSI, with very little change to the user-visible programming interface, the SPE was redesigned and reimplemented to use MPI-1 for communication between processes. The SPE has been distributed to potential users of Windows NT, Sun Solaris, SGI Origin 2000, IBM SP2, and HP V2500 systems, and has been ported to the CSPI-embedded computer. Also, several DoD projects have developed SPE-based scalable, parallel modules. These include Synthetic Aperture Radar (SAR) at SSC San Diego (funded by CHSSI) and Naval Air Systems Command (NAVAIR) Patuxent River (funded by the Programming Environment and Training [PET] Initiative), Automatic Target Recognition (ATR) at Army Research Laboratory Aberdeen, and Active Acoustic Sonar Processing at SSC San Diego.

Significance: With availability on a wide variety of platforms, the SPE has the potential to be the foundation on which parallel, scalable software modules can be provided to the signal- and image-processing community. Because of the SPE's support for modular programming, the various modules can be freely interconnected in much the same style as Khoros. The resulting applications can be directly ported from workstations, to HPC systems, and to any embedded system for which the SPE has been implemented.



Sonar receiver response for successive transmissions when using an autofocus technique on a towed line array. The algorithm adapted for platform dynamics and acoustic propagation provides improved sonar track estimation over conventional navigation instrumentation.

Advanced Virtual Intelligence, Surveillance, and Reconnaissance (ADVISR)

R. A. Pritchard

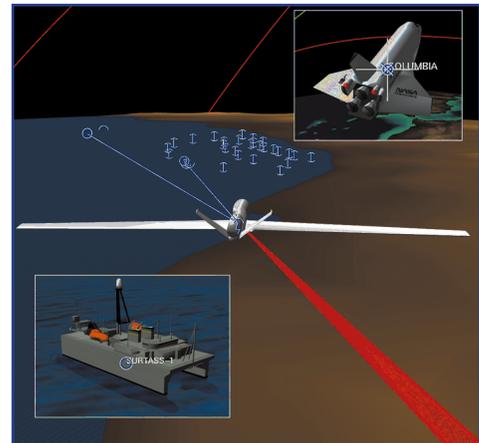
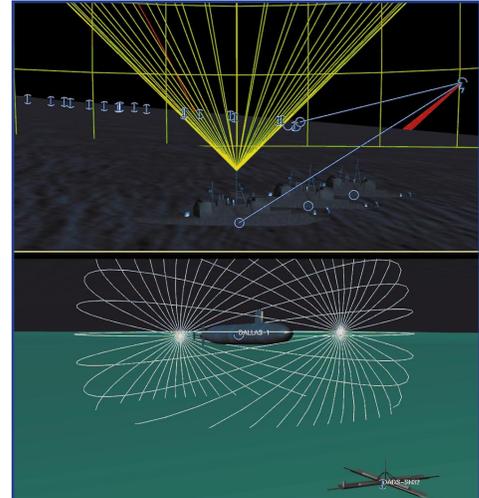
HPC Computer Resource: HP V2500 (SSC San Diego DC)

Research Objectives: Develop scalable, portable, HPC software that provides the capability to design, build, and test systems and metasystems (systems of systems) in virtual reality.

Methodology: HPC and high-bandwidth, low-latency, networking technologies provide a capability to virtual prototype real-time systems and metasystems. Advanced Virtual Intelligence, Surveillance, and Reconnaissance (ADVISR) system elements are designed to be performance and interface equivalent to their real counterparts. Systems can initially be designed, developed, and tested in diverse modes including all-virtual domain and virtual-real combinations. Real-time, physics-based models are used for virtual-reality prototyping of sensor, communication, data-fusion, command and control (C2), and other types of systems. HPC is required for real-time calculation of target tracks; source spectral energies; propagation loss from multiple sources to multiple sensors via multiple paths as a function of frequency; environmental and instrument noise; sensor signal processing, and data fusion. ADVISR includes a real-time, 3-D, round-earth, visualization environment that allows the user to visually correlate and provide multi-aspect views of entity positions and orientations, terrain and bathymetry, raster-map, satellite photo-reconnaissance, and Digital Chart of the World data, as well as nonvisual effects such as antenna patterns, sensor sensitivity volumes, link connectivities, environmental data, and satellite orbits. ADVISR is implemented on a heterogeneous network of machines. The HP V2500 is linked to an SGI Onyx2 visualization computer by a dedicated fiber-optic High Performance Parallel Interface (HIPPI). An asynchronous transfer mode (ATM) switch links the HP V2500 to local classified assets and to other HPC assets, where ADVISR processes can run via the Defense Research and Engineering Network (DREN). System elements and GUIs are implemented as portable and scalable Parallel Virtual Machine (PVM) processes and named mailboxes to allow asynchronous startup and connections.

Results: ADVISR is being used to virtual prototype the Deployable Autonomous Distributed System (DADS). DADS is a wide-area networked field of low-cost sensors that can operate in an undersea environment to detect, locate, classify, and neutralize the quiet submarine as a potentially dominant threat in littoral warfare. Sensor and master nodes are implemented by using Advanced Development Model software stimulated by virtual magnetic and acoustic sensors. Virtual acoustic data links are used for internode communication with virtual RF communication links used to transfer data to real C2 systems.

Significance: Virtual systems can be used to (a) evaluate system concepts and architectures; (b) test and optimize complex systems before building them with external system elements and warfighters-in-the-loop; (c) provide early detection and correction of design and development problems by early testing using specification, design, and measured data, as well as real hardware and software, as available; (d) provide training and mission-rehearsal capabilities; and (e) evaluate the effectiveness of system modifications. ADVISR can also be used to demonstrate the importance of HPC in the simulation of air-traffic-control and in a variety of monitoring systems.



High performance computers provide system virtual prototyping capabilities (screen captures from the ADVISR real-time 3D visualization system).

Parallel Computation of Simulation Objects

Dr. L. J. Peterson and A. Vagus

HPC Computer Resource: SGI Origin 2000 (Navy Research Laboratory [NRL] DC)

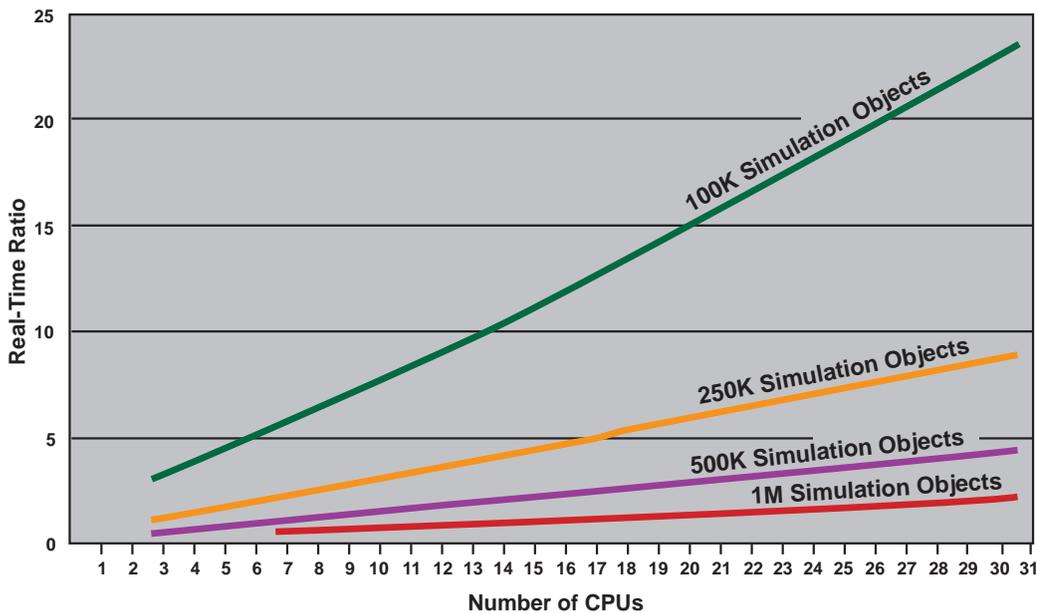
Research Objective: Develop a capability for executing, in faster than real time, a high volume of simulation objects in the range of 100,000 to 1,000,000. The simulation objects are implemented by using the parallel programming language Integrated Modular Persistent Objects and Relation Technology (IMPORT), and the simulation objects are subsequently simulated as discrete events in a high performance computing environment by using the program Synchronous Parallel Environment for Emulation and Discrete-Event Simulation (SPEEDES).

Methodology: Integrate the IMPORT language into the SPEEDES runtime environment. Scalability can then be shown through a demonstration simulation. The simulation consists of three types of objects: one object type represents a Navy Officer giving certain maneuver orders to very high volume fleet ships (i.e., one million ships). Another simulation object is motion—(latitude/longitude with certain direction and speed). The third simulation object is the ship itself. The methodology for implementing these simulation objects uses the parallel programming language known as parallel IMPORT, which has been developed to operate in the HPC environment. The programming language IMPORT is tightly coupled with the program SPEEDES to provide automatic scaling, optimal distribution, and synchronization algorithms required on most defense-specific simulations.

Results: Results show linear performance in increasing the real-time ratio (wall-clock time/simulation time) as one increases the number of CPUs. Also, results show scalability as the number of simulation objects is increased.

Significance: This simple yet powerful test scenario has shown that it is possible to write scalable software using parallel IMPORT when combined with SPEEDES as the simulation engine. What makes it simple to use is that the optimal distribution of data and the use of synchronization algorithms among the CPUs are designed to be transparent to the software engineer writing the application.

This work was done jointly with J. F. Wallace, Epsilon Systems Solutions, Inc.



Scalability of simulation using Parallel IMPORT with 100K to 1M objects on an SGI O2.

Synthetic Aperture Radar Image Formation (SARIF)

C. Yerkes and J. M. Weber

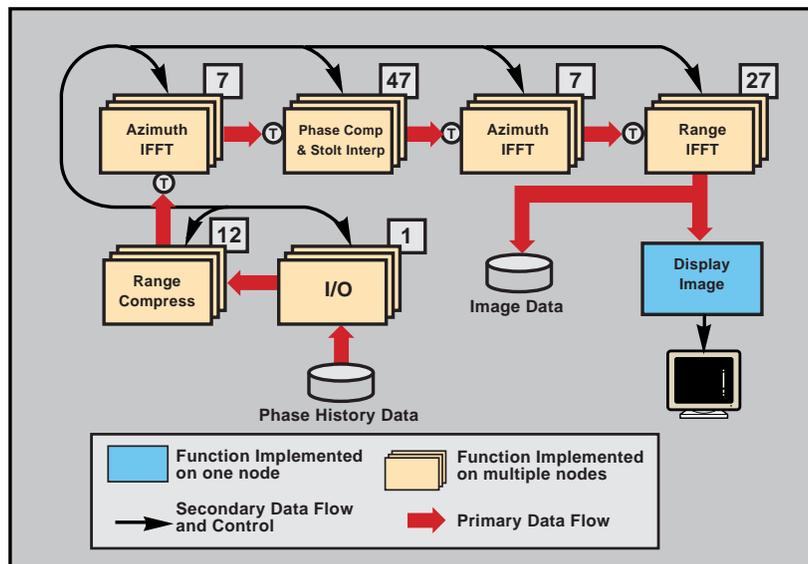
HPC Computer Resource: Intel Paragon (SSC San Diego DC), SGI Origin 2000 (ASC MSRC), IBM SP2 (ASC MSRC), HP V2500 (SSC San Diego DC)

Research Objective: (1) Develop scalable software for Synthetic Aperture Radar (SAR) image formation for DoD surveillance systems by using advanced parallel multidimensional spectral analysis and interpolation techniques. (2) Develop software that is portable across a range of HPC platforms. (3) Demonstrate the effectiveness of modular software techniques in facilitating algorithm enhancements.

Methodology: Three tasks were planned to achieve the CHSSI project goals. A Range Migration Algorithm (RMA) was developed to process UHF/VHF SAR data from sensors currently being used for DoD-funded foliage and ground-penetration research. The process used data from the UHF SAR system operated by SRI International and from the Navy P3 UHF Ultra-Wideband SAR. The second task was the porting and parallelization of a Polar Format Algorithm developed by ERIM, Inc., to various HPC platforms. The Polar Format Algorithm processes X-Band SAR data from the ERIM and Air Force Wright Laboratory Data Collection System SAR. The third task was the development of a middleware software, known as Scalable Programming Environment (SPE), to provide for the parallelism, portability, and modularity of the SAR software.

Results: The CHSSI Range Migration and Polar Format Algorithms were ported to multiple HPC platforms including SGI Origin 2000, IBM SP2, Intel Paragon, HP V2500, and Windows NT. Demonstrations on all platforms were able to show significant scalability of the algorithms. The SPE middleware portion of the software was shown to be reusable in other SAR Automatic Target Recognition (ATR) and non-SAR applications. Also, the SAR algorithms were successfully ported to a CSPI-embedded computer.

Significance: Traditionally, the SAR processors are sequential in execution and take several hours to process the raw data or are only able to process a small portion of the overall data. Also, SAR processors that have been developed for real-time hardware are inflexible and make algorithm enhancement difficult. In contrast, the CHSSI SARIF processors, which have been written for the high performance computers and have been parallelized to take advantage of the scalable software, can produce results in sub-real-time and provide the flexibility to evaluate algorithm enhancements.



The SAR Range Migration Algorithm functional and data flow diagram implemented as a parallel, scalable high performance program. The RMA is portable to multiple HPC platforms and runs on an arbitrary number of nodes selectable by the user.

SSC San Diego Distributed Center

SSC San Diego is one of 17 Distributed Centers established by the DoD High Performance Computing Modernization Program (HPCMP). The SSC San Diego Distributed Center (DC) operates two HPC facilities, one at the classified level and the other unclassified. Each facility currently includes a Hewlett-Packard (HP) V2500 scalable parallel system with 16 PA-RISC processors operating at 440 MHz and with 24-GB memory linked to a storage system with 600-GB disk and 10.5-TB robotic tape storage. High-speed ATM OC-12c (622-Mbits/s) connectivity to these local computers and all other HPC Centers on the Defense Research and Engineering Network (DREN) as well as other national networks is made possible through the SSC San Diego networking infrastructure.

The SSC San Diego DC is in the process of an upgrade that will add HP Superdome systems to the classified and unclassified facilities. Each of these two Superdome systems will be configured with 48 PA-RISC processors operating at 550 MHz and with 48-GB memory. The Superdome machines will be connected to the existing storage subsystems via a Fibre Channel switch, along with the existing V2500 systems.



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